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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/527,580

10/06/2005

Sung-Kyu Hong

8071-80 (OPP 050398 US)

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EXAMINER

NGUYEN, THINH T

ART UNIT

PAPER NUMBER

2818

MAIL DATE

DELIVERY MODE

03/17/2008

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/527,580	Applicant(s) HONG ET AL.	
	Examiner THINH T. NGUYEN	Art Unit 2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 15 November 2007.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-14 is/are pending in the application.
- 4a) Of the above claim(s) 4,10,11,13 and 14 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-3,5-9 and 12 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED OFFICE ACTION

1. claims 1-14 are pending in the Application with claim 4,10-11,13-14 withdrawn from consideration as directed

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this office action.

A person shall be entitled to a patent unless --

(e) the invention was described in-

(1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or

(2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

3. Claims 1-3,5-9,12 are rejected under 35 U.S.C. 102(e) as being anticipated by Kim et al. (US patent 6,936,845) thereafter Kim 845.

The applied reference has a common Assignee and inventors with the instant application. Based upon the earlier effective U.S. filing date of the reference,(noted that the effective filing date in the US of the present Application is March 11th 2005) it constitutes prior art under 35

U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention “by another,” or by an appropriate showing under 37 CFR 1.131.

The Applicant cannot rely upon the foreign priority papers to overcome this rejection because a translation of said papers has not been made of record in accordance with 37 CFR 1.55. See MPEP § 201.15.

With regard to claim 1, Kim 845 discloses (the abstract, fig 13,fig 14) A thin film transistor array panel comprising: an insulating substrate; a plurality of first signal lines formed on the insulating substrate; a plurality of second signal lines formed on the insulating substrate and intersecting the first signal lines in an insulating manner; a pixel electrode formed in a pixel area defined by the intersections of the first signal lines and the second signal lines and including a plurality of subareas (fig 13) partitioned by cutouts and a plurality of bridges connecting the subareas; a first thin film transistor (T3 in fig 14) connected to the pixel electrode; a direction control electrode formed in the pixel area and including a portion overlapping at least one of the cutouts, and a second thin film transistor (T2 in fig 14) connected to the direction control electrode (the connection between the drain of T2 that connect with coupling capacitor) , wherein two long edges of each subarea are parallel to each other and the at least one of the cutouts overlapping the portion of the direction control electrode defines one of two longest edges of the subarea. (fig 13)

With regard to claim 2, Kim 845 discloses (the abstract, fig 13,fig 14)a thin film transistor array panel further comprising a third signal line (the line on fig 14 that connect to

Vd3 and Vd1) intersecting the second signal lines in an insulating manner and including a portion overlapping at least another of the cutouts which is not overlapping the direction control electrode.

With regard to claim 3, Kim 845 discloses (the abstract, fig 13,fig 14)a thin film transistor array panel wherein the third signal line comprises a pair of portions placed between adjacent

With regard to claim 5, Kim 845 discloses (the abstract, fig 13,fig 14)a thin film transistor array panel wherein: the first thin film transistor connects to a relevant one of the first signal lines and a relevant one of the second signal lines, the second thin film transistor connects connected to a previous one of the first signal lines; and a previous one of the second signal lines, and the thin film transistor array panel further comprises a third thin film transistor connected to the previous first signal line, the relevant second signal line, and the pixel electrode.

With regard to claim 6, Kim 845 discloses (the abstract, fig 13,fig 14)a thin film transistor array panel wherein at least one of the bridges are located near a center of the long edges of the subareas and the other of the bridges are located at an edge of the pixel electrode positioned close to the second signal lines.

With regard to claim 7-9, Kim 845 discloses (the abstract, fig 13,fig 14)a thin film transistor array panel wherein the bridges are located at an edge of the pixel electrode positioned close to the second signal lines., wherein at least one of the subareas is chamfered and wherein the cutouts comprise a transverse cutout bisecting the pixel electrode into upper and lower halves

and a plurality of oblique cutouts having inversion symmetry with respect to the transverse cutout.

With regard to claim 12, Kim 845 discloses (the abstract, fig 13, fig 14) a thin film transistor array panel wherein: the oblique cutouts comprise: a first cutout proceeding from an edge of the pixel electrode toward another edge of the pixel electrode to define one of the bridges located between a terminal of the first cutout and the another edge of the pixel electrode; a second cutout proceeding from an edge of the pixel electrode toward the transverse cutout to define one of the bridges located between the transverse cutout and a terminal of the second cutout; and a pair of third cutouts proceeding from edges of the pixel electrode into the pixel electrode and extending along a straight line to define one of the bridges located between the third cutouts.

4. When responding to the office action, Applicants are advised to provide the examiner with the line numbers and the page numbers in the application and/or references cited to assist the examiner to locate the appropriate paragraphs.

5. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the day of this letter. Failure to respond within the period for response will cause the application to be abandoned (see M.P.E.P. 710.02(b)).

6. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d) which papers have been placed of record in the file.

CONCLUSION

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thinh T Nguyen whose telephone number is 571-272-1790. The examiner can normally be reached on Monday-Friday 9:30am-6: 30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Steven Loke can be reached at 571-272-1657.

The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval [PAIR] system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Thinh T. Nguyen/

Patent Examiner

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